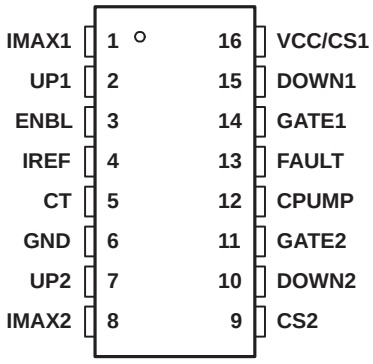
SLVS368 – APRIL 2001

- **Wide Input Operating Range (2.75 V to 13.6 V)**
- **Controls Ramp-Up Sequence and Slope, and Ramp-Down Sequence**
- **Controls Inrush Current**
- **Precise Linear Current Amplifier for High Efficiency and Low Voltage Drop**
- **Programmable Overcurrent Threshold**
- **Programmable Soft-Start Capability and Fault Timer**
- **Internal Charge Pump Drives Low-Cost External NMOS Devices**
- **Cascadable for Three or More Supplies**
- **Fault Indicator Output**
- **Direct-drive of Bus Switch**
- **Shutdown Control with Low-Current Sleep Mode (40 μA)**
- **Input Undervoltage Lockout**
- **16-pin SOIC package**

DW PACKAGE
TOP VIEW



The TPS2306 Hot Swap Power Manager (HSPM) IC provides hot-swap control, fault handling and power supply sequencing of two positive voltage supplies. The TPS2306 operates over a wide supply range allowing single part inventory for a variety of output voltages.

During the transient period of a live insertion or hot-swap event, the TPS2306 actively limits the inrush current to the plug-in module. An on-chip linear current amplifier (LCA) provides closed-loop control of the current sourced to the load circuitry on the module. Subsequently, during normal steady-state loading conditions and in conjunction with an internal high-voltage charge pump, the LCA provides direct gate drive to fully enhance the external NMOS pass devices. In addition, the < 4-mV input offset voltage of the LCA allows for the use of low-value sense resistors. Together, these features minimize the insertion loss across the hot-swap interface.

Control inputs allow the designer to program the maximum current level and the inrush current profile (slew rate) during start-up. Direct programming of the fault time-out also allows the user to establish how long the HSPM can operate in the current control mode prior to turning off the pass elements. The high degree of user programmability allows the TPS2306 to be configured for the specific load and bulk capacitance charging requirements of the target system.

A second level of power bus protection is provided in the form of fast overcurrent comparators monitoring the load current levels of the two channels. Should a short-circuit event's edge rate ever exceed the slew rate of the LCA, the overcurrent comparator immediately latches off the external NMOS devices, overriding the timeout period. The overcurrent threshold is also user-programmable.

Supply sequencing control is provided via four comparator inputs to independently control the ramp-up and ramp-down of each supply output (see Figure 1). The TPS2306 also provides a TTL and CMOS compatible enable input for external control of the supply outputs, and a low-power sleep mode. Also, the open-drain FAULT output provides single-line fault reporting to the system host for the two monitored supplies.

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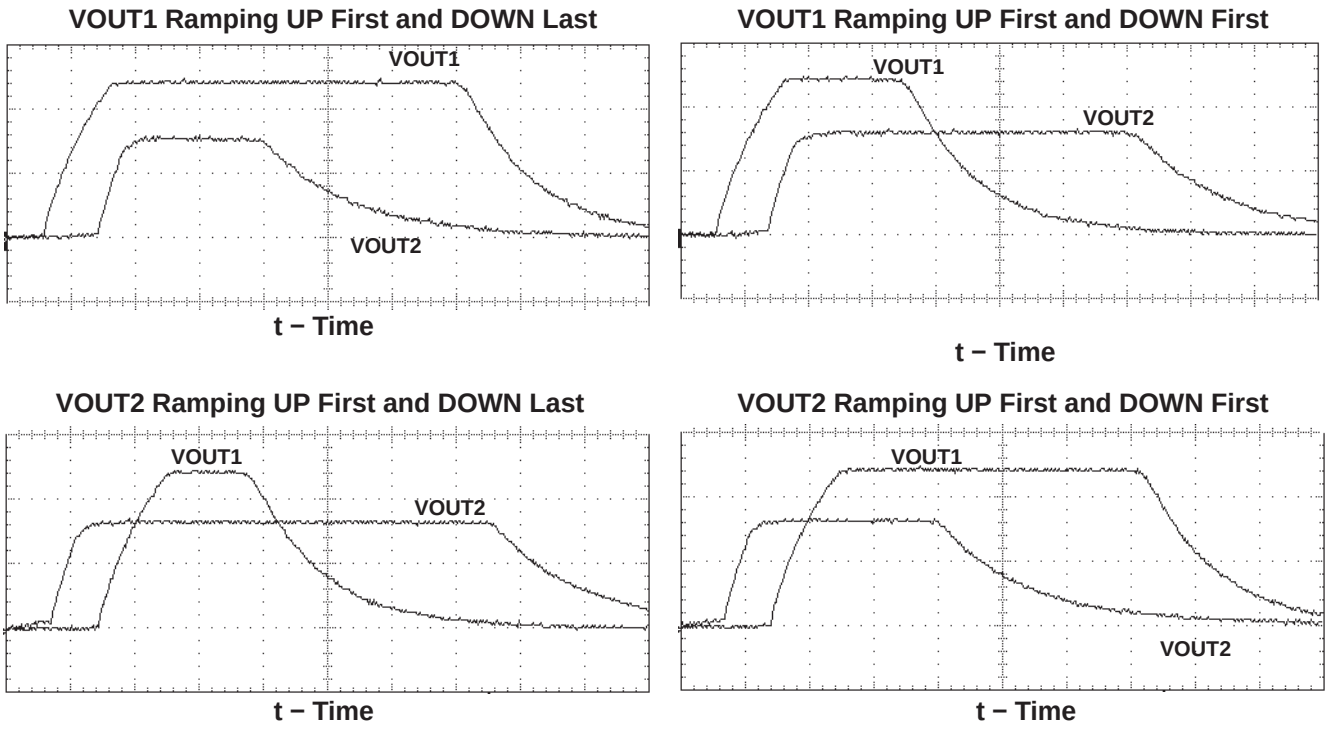


Figure 1. Example Voltage Ramp-up/Ramp-down Sequences

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

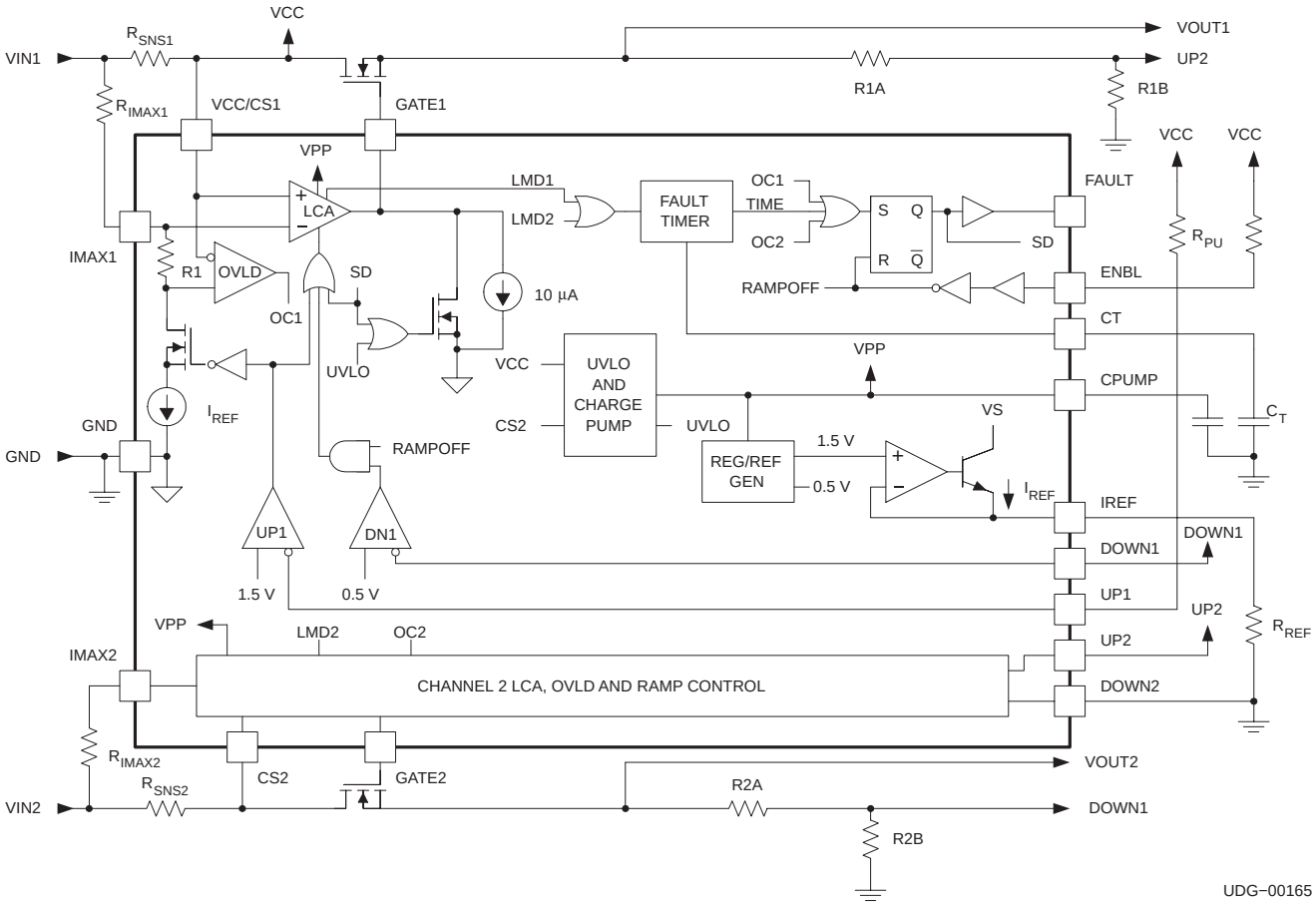
Supply voltage range: VCC/CS1 . . . . . −0.3 V to 15 V
Output voltage range: CPUMP, GATE1, GATE2 . . . . . −0.3 V to 30 V
All others . . . . . −0.3V to VCC+0.3 V
Output current range: I_{REF} . . . . . 0 mA to −1 mA
Operating virtual junction temperature range, T_J . . . . . −55°C to 150°C
Storage temperature range T_{stg} . . . . . −65°C to 150°C
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

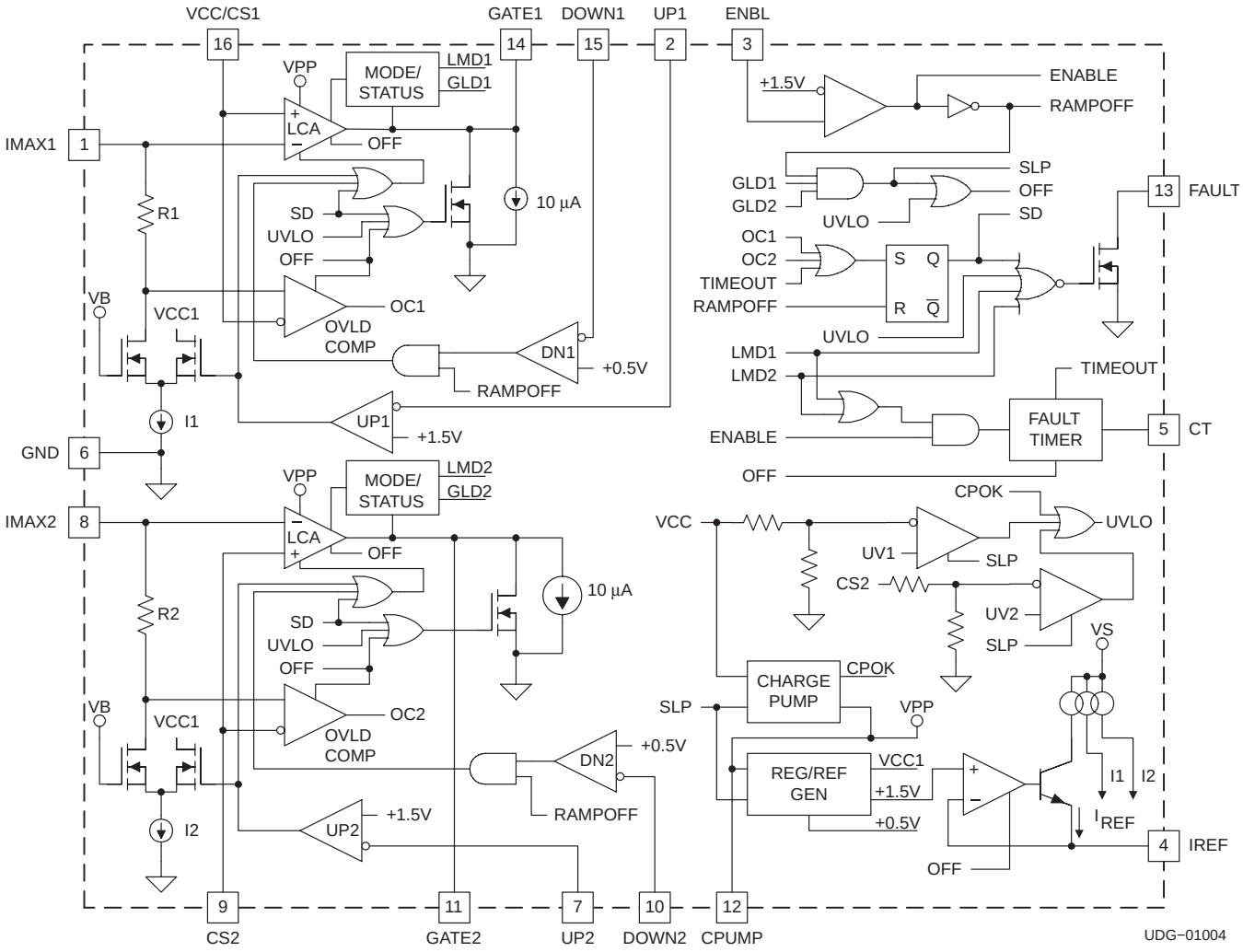
recommended operating conditions

	MIN	MAX	UNIT
Supply voltage (VCC/CS1)	4.0	13.6	V
Input voltage (CS2)	2.75	13.6	V
Output current (IREF)	−300	−35	µA

typical application



functional block diagram



electrical characteristics over recommended operating junction temperature range, $V_{I(VCC/CS1)}$ = 12 V, $V_{I(CS2)}$ = 5 V, −40°C < T_A < 85°C, all voltages are with respect to GND; $T_A = T_J$. (unless otherwise noted) Currents are positive into and negative out of the specified terminal.

input supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Supply current	VCC/CS1 = 4 V, CS2 = 2.75V		1	2	mA
I_{CC2}	Supply current	VCC/CS1 = 13.6 V, CS2 = 13.6 V		2	4	
I_{SLP}	Shutdown current	ENBL = 0		40	75	µA

undervoltage lockout

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC/CS1 minimum voltage to start	CS2 = 3 V	2.00	2.45	2.90	V
VCC/CS1 minimum voltage after start	CS2 = 3 V	1.80	2.25	2.60	
VCC/CS1 hysteresis	CS2 = 3 V	0.05	0.18	0.24	
CS2 minimum voltage to start	VCC/CS1 = 4 V	2.00	2.45	2.75	
CS2 minimum voltage after start	VCC/CS1 = 4 V	1.80	2.25	2.60	
CS2 hysteresis	VCC/CS1 = 4 V	0.05	0.18	0.24	

reference current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	I_{REF} = 100 µA	1.4	1.5	1.6	V
I_O	Maximum output current	V_{REF} = 1.35 V		−300	−150	µA

linear current amplifier 1, linear current amplifier 2

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	T_A = 25°C	−4		4	mV
		−40°C ≤ T_A ≤ 85°C, See Note 1	−5.5		5.5	
I_{PK}	Ouput peak current		−25		−5	mA
I_{SINK}	Output current sink	Ramp-down mode	2	10	25	µA
		LCA pulldown	0.2		5	mA
I_{FAULT}	Output current sink	Overcurrent fault shutdown		100		mA
V_{OL}	Output low voltage	Fault shutdown I_{SINK} = 10 mA			0.5	V
V_{OH}	Output high voltage	I_{SOURCE} = −4 µA	Note 2			V

overcurrent amplifier 1, overcurrent amplifier 2

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	(VCC/CS1 − IMAX1), (CS2 − IMAX2)	Note 3		Note 4	mV
R_{INT1}, R_{INT2}	Internal threshold resistor		1.7	2.5	3.3	kΩ
t_R	Response time		0.5		7	µs

FAULT timer

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CT}	CT charge current	$V_{O(CT)}$ = 1 V	−65	−50	−35	µA
V_{TH}	CT fault threshold		1.35	1.50	1.65	V

NOTES: 1. Ensured by design. Not production tested.
2. V_{CPUMP} − 1
3. $-1.5 \times I_{REF} \times 2500$
4. $-0.6 \times I_{REF} \times 2500$

ENBL input

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage		2			V

FAULT output

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{LKG}	Output leakage current	ENBL = 0 V,	V_{PULLUP} = 5 V			1	μA
V_{OL}	Ouput low voltage	ENBL = 5 V,	I_{SINK} = 0.1 mA			0.5	V
I_{SINK}	Output current sink	ENBL = 5 V,	V_{OL} = 0.5 V		1		mA

charge pump

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Maximum output voltage	I_{CPUMP} = −25 μA		17		25	V
I_{SOURCE}	Maximum current source	VCC= 5 V			−50		μA
Z_O	Charge pump source impedance	VCC= 5 V,	$\frac{(17\ V - 16\ V)}{(I(CP = 17\ V) - I(CP = 16\ V))}$		50		kΩ

ramp-up comparator 1 and ramp-up comparator 2

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UP}	Trip threshold		1.35	1.5	1.65	V

ramp-down comparator 1 and ramp-down comparator 2

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DN}	Trip threshold		0.35	0.5	0.65	V

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CPUMP	12	O	Charge pump output
CS2	9	I	Channel 2 current sense input
CT	5	I/O	Fault timer capacitor pin
DOWN1	15	I	Ramp-down comparator input for channel 1
DOWN2	10	I	Ramp-down comparator input for channel 2
ENBL	3	I	Device enable input
FAULT	13	O	Active high fault indicator output
GATE1	14	O	Pass FET gate drive (output of LCA1)
GATE2	11	O	Pass FET gate drive (output of LCA2)
GND	6	−	Common ground connection for the IC
IMAX1	1	I	Maximum sourcing current programming input for channel 1
IMAX2	8	I	Maximum sourcing current programming input for channel 2
IREF	4	O	Reference current programming pin
UP1	2	I	Ramp-up comparator input for channel 1
UP2	7	I	Ramp-up comparator input for channel 2
VCC/CS1	16	I	Device supply input and channel 1 current sense input

NOTE: Connecting a scope probe or other metering device to the CT pin alters the fault time.

detailed pin description

CPUMP — Charge pump output. A capacitor with a value between 0.01 μF and 0.1 μF must be connected between this pin and ground. The capacitor provides charge storage for driving the gate of the external NMOS device.

CS2 — Channel 2 current sense input. This pin is used as the current sense for the LCA on the second supply controller. This pin must be connected to the sense resistor on the input supply having the lower potential.

CT — Fault timer capacitor pin. A capacitor connected from this pin to ground is used to establish the amount of time that the TPS2306 is allowed to operate in the constant-current mode.

DOWN1, DOWN2 — Ramp-down comparator inputs for Channels 1 and 2, respectively. These inputs are used to sequence the turn-off of the two supply outputs. Each output starts its turn-off when the voltage on the corresponding DOWN*x* input falls below the nominal 0.5 V threshold.

ENBL — Device enable input. Pulling this pin below 0.8 V turns off both external FETs, and puts the IC in low-current sleep mode. Driving this pin above 2.0 V enables the TPS2306.

FAULT — Active high fault indicator output. This pin becomes a high impedance when a latched fault occurs. The indication can be the result of a fault time-out or overcurrent condition on either supply. This output can be used to generate a visual indication of a plug-in card's status, or as an enable signal for a bus isolation switch.

GATE1, GATE2 — Outputs of the linear current amplifiers. These pins are used to drive the gates of the external N-channel FETs which act as switches to either turn ON or OFF input supply current to the two loads.

GND — Common ground connection for the IC.

IMAX1, IMAX2 — Programming input to establish the maximum sourcing current level for each of the supplies. A resistor must be connected between each input supply rail and the corresponding IMAXx input pin of the device. An internal current sink at each of these pins develops a voltage across the programming resistor, providing the reference level or threshold at the inverting input of each LCA.

IREF — Reference current programming pin. An external resistor must be connected between this pin and device ground. Current sourced from this pin determines the precision current sink value at the two IMAXx pins, thus establishing the constant-current and overcurrent thresholds for the application circuit.

UP1, UP2 — Ramp-up comparator inputs for Channels 1 and 2, respectively. These inputs are used to sequence the turn-on of the two supply outputs. Each output begins to ramp up when the voltage on the corresponding UPx input exceeds the nominal +1.5 V threshold.

VCC/CS1 — Supply input for the TPS2306 and channel 1 current sense input. VCC/CS1 is a dual function pin used for input power to the chip, as well as the current sense input for the channel 1 LCA. For proper device operation, VCC/CS1 must be connected to the sense resistor of the input supply having the highest voltage potential.

APPLICATION INFORMATION

detailed description

linear current amplifier

The linear current amplifiers (LCAs) provide closed-loop control over the inrush current during live insertion or remote turn-on. This closed-loop operation provides direct control of the maximum current that is supplied to the load, and allows the user to establish the current transient profile.

The current magnitude information is provided as the voltage drop across a low-value sense resistor at the non-inverting input of the LCA. This voltage is compared to a user-programmable reference at the IMAX*x* inputs. When power is applied to the plug-in card and the device is enabled, the LCA output starts to ramp the voltage of its corresponding MOSFET gate. As the load current increases, the voltage at the CS*x* pin approaches that of the IMAX*x* pin. The LCA servos the GATE*x* output to maintain equal voltages at its inputs. In this mode, the external MOSFET acts as a constant current source at this preset current level, herein referred to as *IMAX*.

Once the bulk capacitance of the load electronics is charged to the input supply level, the inrush current tapers off to the steady-state load level. With decreasing voltage drop across the sense resistor, the voltage at the non-inverting input rises. The LCA then saturates, attempting to drive the GATE*x* output to its supply level. An internal charge pump supplies this drive voltage (VPP in the block diagram) to fully enhance the external FETs.

LCA operation in the linear mode also starts an internal timer (see Fault Timer section). Should the timer expire under a continued constant-current condition, the LCA is disabled, and additional gate discharge paths are turned on to pull the gate low with a nominal 100-mA current. This feature prevents indefinite current sourcing into a faulty load, such as a short-circuit.

The VCC/CS1 input is a dual function pin used for input power to the chip, as well as the current sense input for the channel 1 LCA and overcurrent comparator (OVLD COMP in the functional block diagram). CS2 is the current sense for the LCA and overcurrent comparator on the second (channel 2) supply controller. The CSx sense inputs are connected to the load side of each of the sense resistors. For proper device operation, VCC/CS1 must be connected to the sense resistor on the input supply with the highest potential. CS2 is connected to the sense resistor on the input supply with the lower voltage potential. In typical applications, the device supply current (4 mA maximum at V_{CC} = 13.6 V) is small in relation to the monitored output current, and so has negligible impact on the accuracy of the constant current threshold.

overcurrent comparator

Each supply is also monitored by an overcurrent (or overload) comparator, whose threshold is set relative to the maximum sourcing, or IMAX, limit. The overcurrent comparators provide the electronic circuit breaker function once the LCAs have left the constant-current operating mode and the MOSFET is fully enhanced. The overcurrent thresholds define catastrophic fault current levels. Should a current overload be detected by the device, the LCAs are immediately disabled, and the external FETs turned off, bypassing the fault timer.

The overcurrent comparators are required due to the finite response time required to pull the LCAs out of saturation once the MOSFETs are fully enhanced. If a fault exists when power is initially applied to the board, the LCA starts up in constant-current mode and limits the load current to IMAX until the fault timer expires. The overcurrent comparator does not trip under this condition.

APPLICATION INFORMATION

constant-current source level and overcurrent threshold programming

Constant-current source level and fault level programming is accomplished using the IMAX*x* input pins in conjunction with the IREF pin. An external resistor connected between the IREF pin and ground is used to program the internal reference current to a user-selectable value. As shown in the block diagram, the TPS2306 sources current from the IREF pin to maintain a 1.5-V level at this pin. This current is then mirrored to generate two current sources driving a differential switch on each of the device channels. When the device is enabled, these sources generate a sink current of magnitude (1.1) $\times$ (1.5 V/R_{REF}) at each of the IMAX*x* inputs. Typical values for the programmed reference current are between 35 μA and 300 μA.

External resistors (R_{IMAX1} and R_{IMAX2} in the typical application diagram) connected between the IMAX1 and IMAX2 pins and the corresponding input voltage rails develop a voltage drop relative to that supply potential. This drop programs the current level to be sourced to the load. During constant-current operation, the linear amp slews to limit the voltage across the external sense resistor to the voltage across the corresponding R_{IMAX} resistor, thus limiting the load current.

Slew rate control of the start-up inrush current (soft-start), is easily achieved with the addition of a capacitor across the IMAX programming resistor (C_{SS1} and C_{SS2} in the Figure 2 application diagram). This applies an RC time constant to the ramp-up of the voltage at the IMAX pin, and a corresponding RC characteristic on the inrush transient during ramp-up of the output voltages. Since the IMAX*x* pin current sink is off until each channel is commanded ON by the UP*x* comparators, the soft-start cap remains discharged until turn-on, regardless of whether start-up is due to a live insertion event, or remote turn-on of a unit whose supply inputs have been charged indefinitely. No additional soft-start reset components are required.

The overcurrent comparator thresholds are established in a similar manner, except that an internal fixed resistor sets the overcurrent threshold (see R1 and R2 in the block diagram). The IMAX programming current also flows through the overcurrent threshold resistors, generating a reference level that is offset from the corresponding IMAX reference. These internal resistors have a nominal 2.5-kΩ value, so the comparator thresholds are a nominal (2500 $\times$ I_{REF}) V above the fault threshold. Note that since the reference current is programmable, the user has modest control of the overcurrent threshold for a given sense resistor value.

supply sequencing

Control of both the power up and power down sequence of the two supplies is provided via the four sequencing inputs, UP1, UP2, DOWN1, and DOWN2. Each channel's external pass element is ramped on when the ENBL input is asserted, and the voltage at the corresponding UP*x* pin exceeds the nominal 1.5-V reference threshold. The turn-off of the two supplies may also be initiated via the ramp-up comparators; however, for more autonomous operation, the DOWN*x* inputs are used. When the device ENBL signal is deasserted, the outputs of the ramp-down comparators (DN1 and DN2) are gated to the LCA control logic (see block diagram). When the voltage at either DOWN*x* input drops below a nominal 0.5 V, that channel's LCA is disabled, and the pass element's gate is subsequently discharged by a 10-μA pull-down current.

APPLICATION INFORMATION

charge pump and housekeeping

The TPS2306 contains an on-chip high-voltage charge pump circuit to step up the supply potential at the VCC input to provide the gate drive for external N-channel devices. A capacitor with a value between 0.01 μF and 0.1 μF must be connected from the CPUMP pin to ground to provide additional energy storage on the charge pump output.

During a start-up sequence, undervoltage lockout (UVLO) comparators monitor the supply levels at the VCC/CS1 and CS2 pins, as well as the charge pump output. The LCAs are inhibited, and the GATE*x* outputs pulled low, until input and charge pump levels exceed the UVLO threshold levels. This ensures sufficient supply potential for the device and LCAs for predictable sequencing control, fault detection, and gate drive prior to turning the outputs on. The VCC/CS1 input UVLO threshold has a maximum specification of 2.9 V to ensure start-up, down to the minimum recommended operating supply of 4.0 V. The CS2 input starts with a 2.75-V input level. There is a nominal amount of hysteresis on the input thresholds to guard against repeated starts in response to supply droop. The charge pump UVLO threshold is set for a nominal 12.5 V with a V_{CC} input of 5 V.

fault timer

The fault timer block contains the control circuitry for generating a time delay, which determines how long the TPS2306 is allowed to operate in the constant-current, or linear, mode. Without the timer, fault conditions such as starting up into a shorted load, would cause the TPS2306 to operate in the constant-current mode indefinitely, at the programmed IMAX sourcing level. Conversely, the HSPM must allow sourcing long enough to charge the input bulk capacitance. The determination of the time period needed depends on several factors, including:

1) the amount of capacitance to be charged, 2) the load characteristic (constant-current or resistive), and 3) the soft-start characteristic, if used. Information about estimating the required timeout period is provided in the Application Information section.

The fault time-out needed is the total ramp-up time of the two channel outputs.

Setting of the user-programmable time-out period is accomplished by connecting a capacitor between the device CT pin and ground. When either of the linear amplifiers is operating in constant-current mode, circuitry in the MODE/STATUS block generates the corresponding linear mode detected (LMD*x*) signal, starting the timer. The timer operates by sourcing a nominal 50-μA from the CT pin, charging the external capacitor from 0 V. If output charging completes prior to time-out, the LCA's drive to the rail, and load sourcing continues uninterrupted. However, if the constant-current mode persists until the timing capacitor voltage exceeds the 1.5-V fault threshold, the TIMEOUT signal is latched as the shutdown signal (SD in the block diagram). Both FET switches are turned off, and the FAULT output remains asserted.

To restart from a fault timeout, either the ENBL input must be toggled LO then HI, or device power must be cycled.

enable input

The ENBL input allows host or remote turn-on and turn-off of the controlled supplies. Pulling this pin below 0.8 V disables both external NMOS devices, and puts the IC in low-power sleep mode. Driving this pin above 2.0 V enables the supply outputs. Because of the level translation circuitry at the ENBL input, this pin may be pulled up externally to the V_{CC} rail. As seen in the block diagram, assertion of the sleep mode (SLP) signal turns off much of the peripheral circuitry of the device, including the charge pump, references, LCAs and overcurrent comparators, reducing supply current to only 40 μA typical with V_{CC} = 12 V. In order to ensure controlled shutdown according to the configured sequencing scheme, the gate potential of each output is monitored by the MODE/STATUS circuitry. Once both gates have discharged below 1 V, the gate low detect (GLD*x*) signals allow the part to enter sleep mode.

APPLICATION INFORMATION

fault output logic

The FAULT signal is an open-drain output which is high-impedance under any conditions which cause the outputs to be switched off, including an overcurrent or fault time-out on either supply, removal of the external enable signal with subsequent GATE*x* ramp-down, or an undervoltage condition on either supply input. Refer to the Application Information section for additional details on using this output.

The circuit diagram of Figure 2 shows a dual hot-swap application in which the TPS2306 is used to hot swap and sequence 5.0-V and 3.3-V supplies. The total input bulk and filter capacitance associated with the +5.0V load is represented in the diagram by C_{LOAD1}. C_{LOAD2} represents the load capacitance on the 3.3 V supply. The nominal operating currents of each load are represented by the I_{L1} and I_{L2} blocks.

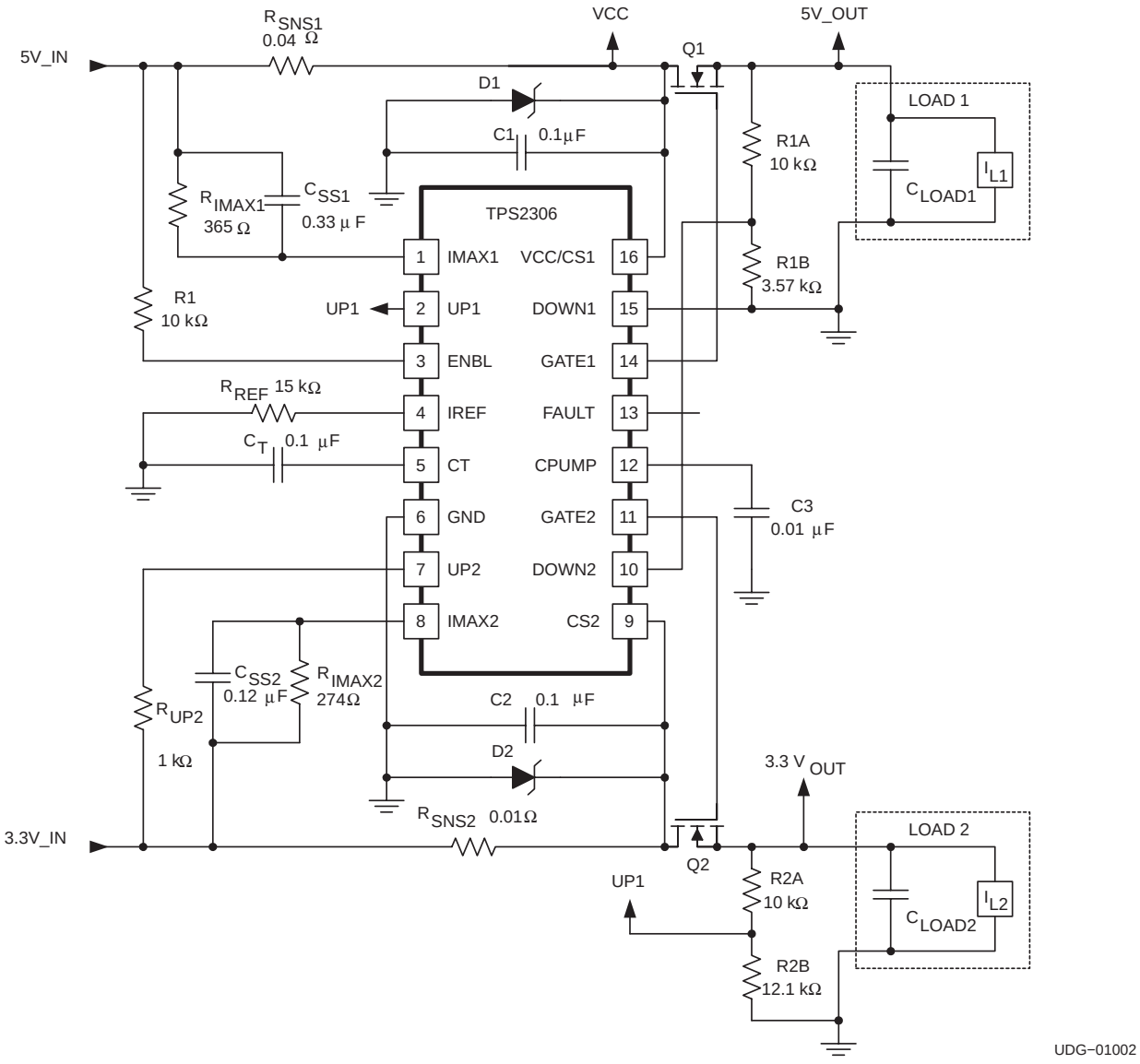


Figure 2. TPS2306 in a 5-V/3.3-V Dual Hot Swap Application

APPLICATION INFORMATION

Note that the 5.0-V supply, being the higher input potential, is controlled by channel 1 of the device; its current sense resistor R_{SNS1} is tied to the VCC/CS1 input, and the FET switch Q1 gate is driven by the GATE1 output. The 3.3-V supply is controlled by channel 2.

In this application, the TPS2306 is connected such that the 3.3-V supply is ramped up first, followed by the 5.0-V supply. A pull-up resistor connected to the 3.3-V input (R_{UP2}) enables this supply ramp when 3.3-V power is applied and the ENBL input is pulled above its 2.0-V ON threshold. A divider on the channel 2 output (R2A and R2B in Figure 2) monitors the $3.3V_{OUT}$ node, and establishes the output level at which the channel 1 supply is allowed to start ramping up.

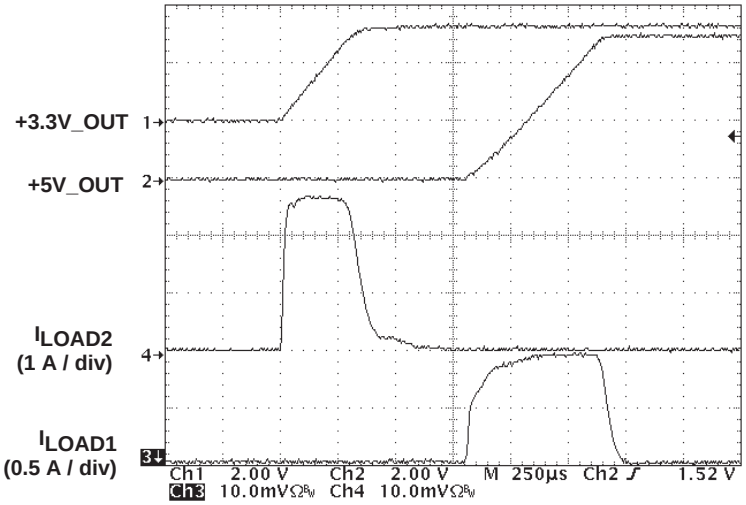


Figure 3. TPS2306 Output Ramp Operation in Figure 2 Circuit.

For ramp-down control, the DOWN1 input has been tied to ground; whereas the DOWN2 input monitors the 5.0-V_OUT status via the R1A/R1B divider net. When the ENBL input is pulled low, channel 1 is turned off first, and the Q1 gate discharged by a nominal 10-µA pull-down. Once the gate has sufficiently discharged, the 5.0-V_OUT node starts to decay according to the LOAD1 characteristic. When the DOWN2 input eventually decreases below the 0.5-V threshold of the DN2 comparator, that gate drive is also turned off. The 3.3-V_OUT node subsequently decays according to the LOAD2 characteristic.

APPLICATION INFORMATION

protecting the TPS2306 from voltage transients

Parasitic inductance associated with the power distribution can cause voltage spikes on the supply inputs if the load current is suddenly interrupted by the TPS2306. It is important to limit the peak of these spikes to less than 15 V to prevent damage to the TPS2306. These spikes can be minimized by:

- Reducing power distribution inductance by locating the supply close to the plug-in module, maximizing the width of high-current traces and using a PCB ground plane.
- Decoupling the VCC/CS1 and CS2 inputs with capacitors (C1 and C2 in Figure 2), located close to the device. These capacitors are typically valued between 0.1 μF and 1.0 μF in a ceramic dielectric.
- Clamping the voltage at the VCC/CS1 and CS2 inputs with Zener diodes (D1 and D2 in Fig.2). The Zener voltage of these devices can be selected according to the nominal input supply levels; however, the maximum breakdown in all cases should be less than 15 V to avoid damage to the TPS2306.
- For applications with high trip currents or significant parasitic inductance, it may be necessary to install additional bulk capacitance on the backplane side of the plug-in interface. These low-ESR capacitors should be physically located close to the plug-in slot connector on the power rails. These devices have the dual benefit of limiting the magnitude of spikes applied to the TPS2306, and limiting supply transients propagated to other modules in the system if one of the protected outputs is interrupted.

layout considerations

Care should be taken to use good layout practice with the parts placement and etch routing of the plug-in PCB to optimize the performance of the hot-swap circuit. Some of the key considerations are listed here.

- Decoupling capacitors should be located close to the device. Keep trace lengths from the capacitor to the current sense input (CS*x*), and to the device GND pin to a minimum.
- Any protection devices (e.g., D1 and D2 in Figure 2) should be located close to the HSPM IC.
- Mount the charge pump reservoir capacitor (C3 in Figure 2) close to the device CPUMP pin.
- The reference current programming resistor (R_{REF} in Figure 2) should be placed as close as feasible to the device, with minimized trace length to the pin 4 output.
- To reduce insertion loss across the hot swap interface, use wide traces for the supply and return current paths. A power plane can be used for the supply return or GND node.
- Additional copper placed at the land patterns of the sense resistors and pass FETs can significantly reduce the thermal impedance of these devices, reducing temperature rise in the module and improving overall reliability.
- Because typical values used for current-sense resistors can be so low (between <10 mΩ and approximately 100 mΩ), board trace resistance between elements in the supply current paths becomes significant. To achieve maximum accuracy of the constant-current thresholds, good Kelvin connections to the resistors should be used for the IMAX and current sense inputs to the device (see Figure 4). The current sense traces should connect symmetrically to the sense-resistor land pattern, in close proximity to the element leads, not upstream or downstream from the device.

APPLICATION INFORMATION

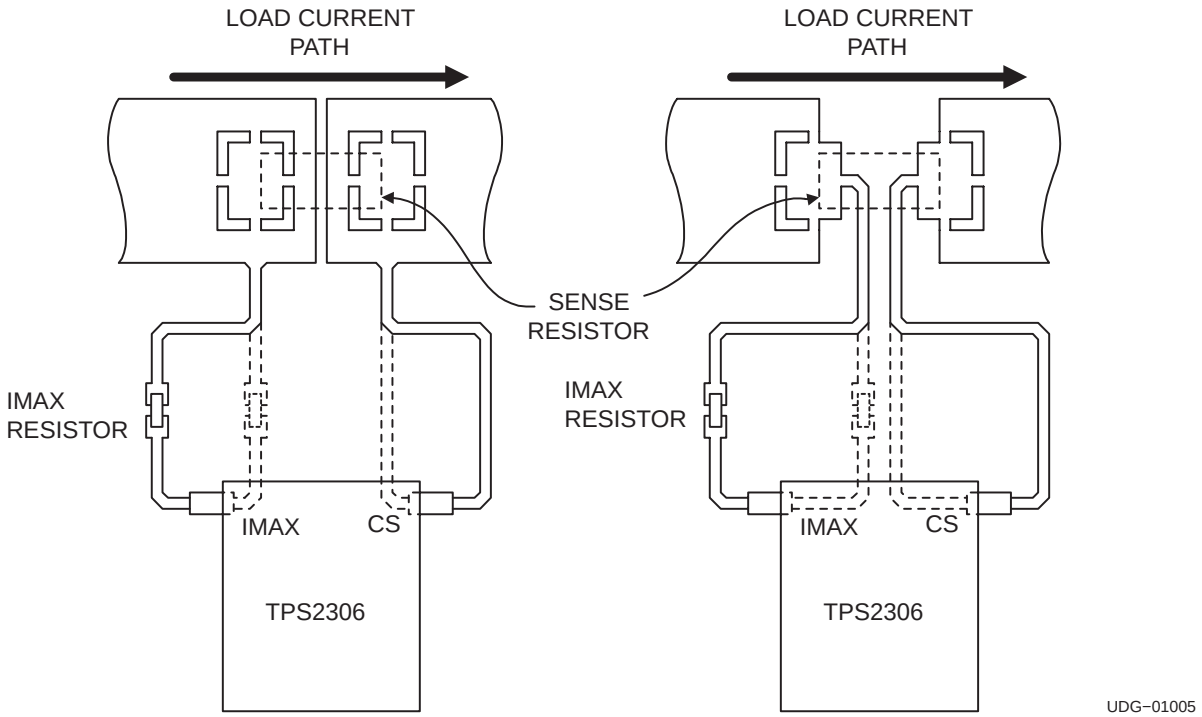


Figure 4. Connecting to the Sense Resistors—SMD Chip

output ramp operation

During a live insertion event, the primary functions of the TPS2306 are to control the inrush current to the two protected loads, and to control the ramp-up sequence of the supply voltages. Inrush control is achieved via the two LCAs, as described in the *Detailed Description* section. To further refine the current limit function, a two-step gate drive sequence is used to drive the external FETs any time the outputs are ramped up. The plot of Figure 5 demonstrates the TPS2306 operation by showing the typical turn-on characteristic at the IMAX1 input.

APPLICATION INFORMATION

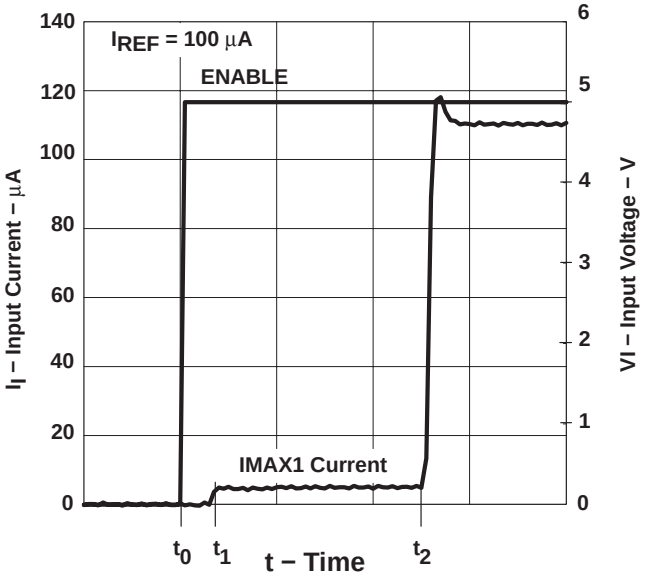


Figure 5. TPS2306 Typical IMAX1 Turn−on Sequence

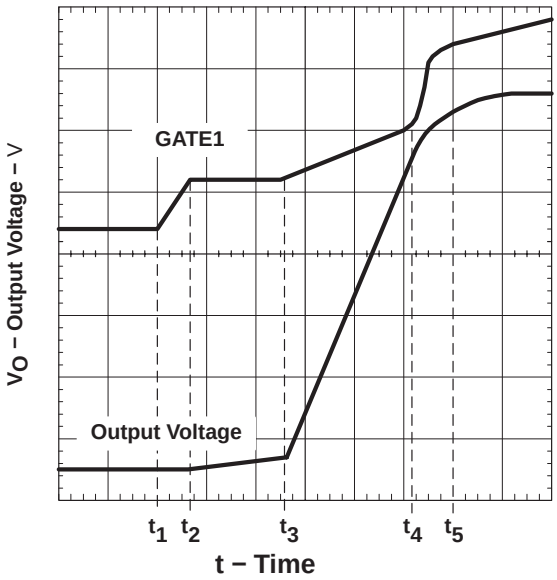


Figure 6. TPS2306 Slow Ramp Operation

In Figure 5, the channel 1 ramp-up conditions are met at time t_0 = 0. This means that the ENBL input is asserted, both supply input and charge pump UVLO conditions are met, and the UP1 input voltage exceeds the 1.5-V threshold. After a nominal delay, the IMAX1 current sink is turned on at t_1, but only at a level that is approximately 5% of the programmed IMAX level. This stage typically lasts approximately 500 μs. After about 500 μs at t_2, the IMAX1 current ramps to the full programmed level ($\cong I_{REF}$).

The same two-step characteristic is also used to turn-on the channel 2 FET.

From the load's perspective, the slow turn-on of the pass elements has the effect shown in Figure 6.

Figure 6 shows the GATE1 and output voltage response to the typical IMAX1 ramp shown in Figure 5. In this example, the FET is driving an RC-type load. At time t_1, the IMAX1 input is turned on at a magnitude of $\cong I_{SNK}/20$. The GATE1 output begins to drive the FET gate. However, the FET remains OFF initially, and no current is allowed to flow. At t_2 the gate voltage exceeds the $V_{GS(on)}$ threshold of the FET. Between t_2 and t_3 the output current is limited to the slow turn-on level established by the TPS2306. Accordingly, only slight charging of the output is obtained during this period. At t_3, the slow ramp time period expires (the current at IMAX1 steps to the programmed level) and the output now charges at a rate of IMAX/C_{LOAD1}. As the output voltage approaches the input supply level around time t_4, the charging current begins to taper toward the steady-state load level. The GATE1 output then drives towards the charge pump voltage, thus fully enhancing the external pass FET. By time t_5, the output has charged up to 95% of the input dc potential.

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Note that the relative occurrence of time t_2 within the t_1 to t_3 window is influenced by a number of factors. Large input capacitance and higher ON thresholds of the external FET delay turn-on of the FET, resulting in reduced output ramp during the first stage. For the TPS2306 parameters, a higher source impedance, smaller slow ramp current, and a shorter slow ramp period (t_1 to t_3) all act to reduce the output ramp during this period. Under some conditions, it's possible that only imperceptible voltage ramping occurs during the slow ramp period, in which case all significant output charging occurs after time t_3.

determining component values

To demonstrate the process of determining the programming component values for a TPS2306-based hot swap circuit, a design procedure is detailed here to show the derivation of the values used in the Figure 2 schematic. For this example, the following system specs were established:

- V_{IN1} = 5.0 Vdc ± 10% V_{IN2} = 3.3 Vdc ± 5%
- C_{LOAD1} = 100 µF C_{LOAD2} = 300 µF
- I_{L1} = 0.50 A I_{L2} = 1.5 A
- IMAX1 = 1.0 A IMAX2 = 3.0 A

The IMAX1 and IMAX2 currents are the constant-current mode sourcing levels that are used for fast charging of the load input capacitance during start-up of the two hot swap channels. To avoid unexpected interruption of the supply currents during normal loading conditions, the constant-current levels must be set above the anticipated load current values.

setting the sense resistor values

The sense resistors are used to feed the load current information back to the TPS2306 LCAs and overload comparators. The values of these resistors can be set by considering the resultant drop under normal (steady-state) loading conditions. For the Figure 2 application, the drop was limited to 20 mV on each channel. Given nominal loading conditions, the sense resistors should be set as follows.

$$R_{SNS1} = \frac{V_{DROP1}}{I_{L1}} = \frac{20\ mV}{0.5\ A} = 40\ m\Omega \quad (1)$$

and

$$R_{SNS2} = \frac{V_{DROP2}}{I_{L2}} = \frac{20\ mV}{2.0\ A} = 10\ m\Omega \quad (2)$$

where:

- V_{DROP1}, V_{DROP2} = the target voltage drop under nominal loading conditions
- I_{L1}, I_{L2}= the respective load currents of each channel

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setting the reference current magnitude

The reference current level is established by connecting a resistor between the TPS2306 IREF pin and ground (R_{REF} in Figure 2). The IMAX*x* sink currents used to develop the constant-current thresholds are determined by this reference current value. The TPS2306 can be configured to source from approximately 35 μA to 300 μA. At 100 μA or greater, the variation in sink currents at the IMAX*x* inputs is typically ±10% of the programmed value; however, variation increases with reference current decreasing below the 100-μA level. In addition, the circuit breaker trip threshold is also established as a resistor drop below the LCA reference (see R1 and R2 in functional block diagram). It is also then a function of the reference current. Therefore, constant-current mode accuracy must be balanced against the circuit breaker trip threshold when establishing design values. For a given sense resistor value, higher values of reference current result in higher overload current thresholds. The circuit breaker setting can be adjusted downward by decreasing the reference current, or returning to the previous step and increasing the value of the sense resistor.

For the Figure 2 application, the reference current was set to 100 μA to maintain current source accuracy. The programming resistor value is then determined from:

$$R_{REF} = \frac{V_{REF}}{I_{REF}} = \frac{1.5\ V}{I_{REF}} \tag{3}$$

where:

- V_{REF} = the IREF pin output voltage
- I_{REF} = the desired reference current

For I_{REF} = 100 μA, the resistor R_{REF} was set to the standard 1% value of 15.0 kΩ.

determining the IMAX programming resistor values

During a start-up sequence, the internal LCAs slew the GATE*x* outputs to maintain the voltage at the CS*x* pins equal to the voltage at the corresponding IMAX*x* input. Therefore, the voltage across the sense resistor R_{SNSx} is equal to the drop across the IMAX*x* programming resistor. Since the sense voltage is the I-R drop of the load current, the R_{IMAXx} resistors can be calculated from:

$$R_{IMAXx} = \frac{IMAXx \times R_{SNSx}}{(1.1) \times I_{REF}} \tag{4}$$

where:

- IMAX*x* = the desired constant-current sourcing level

Substituting values from the example application, the following resistor values were calculated.

$$R_{IMAX1} = \frac{(1.0\ A) \times (0.04\Omega)}{(1.1 \times 100\ \mu A)} \cong 364\ \Omega \quad \text{and} \quad R_{IMAX2} = \frac{(3.0\ A) \times (0.01\Omega)}{(1.1 \times 100\ \mu A)} \cong 273\ \Omega$$

The standard 1% values of R_{IMAX1} = 365 Ω and R_{IMAX2} = 274 Ω were selected.

Again, the constant current levels must be above the nominal operating current of the load electronics for proper operation of the hot swap circuit. Once the sense resistor and IMAX resistor values have been established, this guideline can be verified by testing for the minimum value of the constant-current level, or $IMAXx_{(min)}$. The two main contributors to device-to-device IMAX variance are the tolerance of the IREF output voltage, and that of the current sinks at the IMAX*x* inputs. Assuming the 10% tolerance on IMAX described in the *Setting the Reference Current Magnitude* section, the minimum sourcing current during linear operation can be estimated from equation 5 or 6.

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$$IMAXx_{(min)} \cong \frac{\left(R_{IMAXx}\right) \times (0.9) \times I_{SINK(min)} - V_{OS}}{R_{SNSx}} \quad (5)$$

$$IMAXx_{(min)} \cong \frac{\left(R_{IMAXx}\right) \times I_{REF(min)} - V_{OS}}{R_{SNSx}} \quad (6)$$

where:

- $IMAXx_{(min)}$ = the minimum constant-current level
- V_{OS} = the maximum input offset of the linear current amplifier, ±4 mV
- $I_{REF(min)}$ = the minimum reference current value, determined from $I_{REF(min)} = 1.4\ V/R_{REF}$

Substituting the device and design example values into equation 6, the values of $IMAX1_{(min)}$ = 0.75 A and $IMAX2_{(min)}$ = 2.16 A are obtained, which should provide sufficient margin above the nominal 0.5-A and 1.5-A loads.

Note that in equations 5 and 6 the tolerances of external resistors are ignored; the user can include these if desired.

circuit breaker trip points

At this point in the design process, sufficient information is known to calculate the circuit breaker trip thresholds. Referring to the typical application diagram, the current-sense measurement is applied to the inverting input of the OVLD comparator. It can also be seen from the diagram that the reference voltage for comparison is developed by sourcing I_{REF} through programming resistor R_{IMAX} and the internal resistor R1 (for channel 1). Therefore, the nominal trip current threshold, I_{FLT}, can be calculated from equation 7.

$$I_{FLTx} = \frac{\left(R_{IMAXx} + R_{INT}\right) \times (1.1) \times I_{REF}}{R_{SNSx}} = \frac{\left(R_{IMAXx} + 2500\Omega\right) \times (1.1) \times I_{REF}}{R_{SNSx}} \quad (7)$$

If the resultant circuit-breaker thresholds are determined to be too high, they can be adjusted by a combination of decreasing the reference current and/or increasing the sense resistor value.

soft-starting the TPS2306

Inrush current slew rate control, or soft-start, can be programmed into the TPS2306 operation by adding a capacitor in parallel with the IMAX resistor, as shown by C_{SS1} and C_{SS2} in the Figure 2 schematic. When the output ramp-up is enabled, the IMAX*x* pin voltage ramps with an RC characteristic. Accordingly, the current supplied during output charging (after the initial slow turn-on period) is of the form:

$$I_{SRC}(t) = IMAX \times \left[1 - e^{\left(\frac{-t}{R_{IMAX} \times C_{SS}}\right)}\right] \quad (8)$$

where IMAX is the steady-state constant-current level set by R_{IMAX} if soft-start were not employed, and (from equation 4) is given by equation 9.

$$IMAX = \frac{R_{IMAX} \times (1.1) \times I_{REF}}{R_{SNS}} \quad (9)$$

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If a desired maximum slew rate is known, it can be used to set the value of the soft-start cap, C_{SS}. Since soft-start is $\partial i/\partial t$ control, the required value of C_{SS} can be determined by taking the derivative of equation 8 at time t = 0 and solving for C_{SS}. The result is equation 10 below.

$$C_{SSx} = \frac{IMAXx}{\left(R_{IMAXx} \times \left(\frac{\partial i}{\partial t}\right)_x\right)} \quad (10)$$

where:

$(\partial i/\partial t)_x$ = the desired inrush slew rate of channel *x*

Continuing with the Figure 2 example, if the 5.0-V supply-current ramp is limited to 10 mA per microsecond, but the 3.3-V input is capable of 100 mA per microsecond, the soft-start caps should be set to:

$$C_{SS1} = \frac{1.0\ A}{\left(365\ \Omega \times \left(\frac{0.01}{10^{-6}}\right)\right)} \qquad C_{SS2} = \frac{3.0\ A}{\left(274\ \Omega \times \left(\frac{0.1}{10^{-6}}\right)\right)}$$

$$C_{SS1} \cong 0.27\ \mu F \qquad C_{SS2} \cong 0.11\ \mu F$$

Generally, selecting the next higher available value helps compensate for variations in the actual IMAX levels, such that the $\partial i/\partial t$ does not exceed the design value, even for a hot swap solution operating at the high end of its IMAX tolerance band.

programming the supply sequencing

The TPS2306 makes use of four on-chip comparators to control the ramp-up and ramp-down sequencing of power delivery to the two loads. The UP1 and UP2 inputs are available to configure the ramp-up sequence of Channels 1 and 2 respectively. The functional block diagram shows that the UPx comparators' outputs switch the internal current sources I_1 and I_2 to their respective IMAX*x* pins. In addition, they release disable inputs to the LCAs, enabling LCA drive of the external FET gates.

Output turn-off is programmable via the DOWN1 and DOWN2 inputs. Again referring to the block diagram, when the external enable signal is removed from the ENBL input, the DN*x* comparator outputs are gated to the LCA control logic. When the voltage at either comparator input falls below the 0.5-V reference, that channel's LCA is disabled, removing the gate drive. A nominal 10-μA current source pulls the gate toward the GND pin potential, ultimately turning off the external FET.

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One method of using the UP*x* and DOWN*x* inputs to control sequencing is to use resistor dividers across the loads to sense load status. The dividers scale the output voltages to set the desired value at which controlled channel should ramp up or turn off. In the Figure 2 application, the pull-up on the UP2 input causes the 3.3-V supply to ramp up first, when the enable and input conditions are met. Resistors R2A and R2B form a divider on the 3.3V_OUT node; as this output ramps up, its status is fed back to the UP1 input to control the turn-on of the 5.0-V output. From the diagram, it can be seen that the voltage at the UP1 pin can be determined from the simple divider equation; therefore, the value of the R2B resistor (the bottom leg of the divider) can be selected from:

$$R2B = \frac{V_{UP}}{\left(V_{RAMP} - V_{UP}\right)} \times R2A \tag{11}$$

where:

- V_{UP} = the UP*x* comparator reference voltage
- V_{RAMP} = the desired output voltage of the primary channel at which the secondary channel starts to ramp

The maximum threshold specification can be used to set the maximum output level at which the second channel is enabled. In this case, equation 11 becomes:

$$R2B = \frac{1.65\ V}{\left(V_{RAMP} - 1.65\ V\right)} \times R2A \tag{12}$$

For the example application, the 5.0-V supply is to be ramped after the 3.3-V supply has nearly attained its steady-state level. To ensure operation over the supply tolerance window, this voltage was set to a maximum of 3.0 V. If R2A is set to 10 kΩ, the value R2B = 12.2 kΩ results from equation 12. If the standard value of 12.1 kΩ is selected, the channel 1 output starts ramping at a nominal voltage of:

$$V_{RAMP} = \left(\frac{22.1\ k\Omega}{12.1\ k\Omega}\right) \times 1.5\ V \cong 2.74\ V \tag{13}$$

Similarly, the turn-off threshold for channel 2 is determined by the R1A/R1B divider equation. In this example, DOWN1 was tied low (to ground) to turn off the 5.0-V supply when the enable is deasserted. As the 5.0V_OUT node decays, its status is fed back to the DOWN2 input. Therefore, a resistor value for R1B can be found from:

$$R1B = \frac{V_{DN}}{\left(V_{OFF} - V_{DN}\right)} \times R1A \tag{14}$$

where:

- V_{DN} = the DN*x* comparator reference voltage
- V_{OFF} = the desired voltage of the turn-off control channel at which the controlled channel gate drive is turned off

If R1A is set to 10 kΩ, and channel 2 turn-off should be after the +5.0V_OUT node has decayed to less than 2.50 V, then equation 14 becomes:

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$$R1B = \frac{0.65\ V}{(2.5\ V - 0.65\ V)} \times 10k\Omega \cong 3.51\ k\Omega \quad (15)$$

estimating the output ramp-up time

As described in the *Fault Timer* section, TPS2306 operation in linear mode is limited to the timeout period established by the external capacitor on the CT pin. This timeout must be long enough to allow for either the concurrent or sequential charging of BOTH outputs to the input supply levels. Therefore, an estimate of this ramp-up time is required to ensure start-up.

The output voltage ramp profiles are influenced by a number of factors, including the amount of load capacitance, the load current level, the load characteristic (either resistive or constant-current), and the current ramp profile. Therefore, determination of the charging, or start-up, time is organized into several different load categories:

1. resistive loads, no soft-start
2. constant-current loads, no soft-start
3. constant-current loads, with soft-start

The case which most closely describes the application characteristics should be selected.

> **NOTE:** In the following discussion, the subscripted “1” and “2” suffixes refer respectively to the first channel to ramp up (primary or master), and the second (or controlled or slave) channel to ramp, not necessarily device Channels 1 and 2.

case 1: resistive loads, no soft-start

When the output ramp conditions are met, the pass FET gates are initially only driven to source a current of approximately 5% of the IMAX current to the loads, as described in the *Output Ramp Operation* section. This first step lasts a nominal 500 μs. Subsequently, the output current is ramped to the full IMAX setting. For typical applications, the extent of capacitance charging during this slow ramp period is relatively small. Therefore, it can be neglected in estimating total start-up time, simplifying calculations. However, since the HSPM timer is started as soon as the first output starts ramping, the slow ramp period is included as a component of the total ramp-up time.

Given these considerations, the start-time calculation approximates the source as making a step change from 0 to IMAX, once enabled. Therefore, the time for either output to charge to a given voltage, $v_x(t)$, can be found from:

$$t = R_{Lx} \times C_{Lx} \times \ell n \left[\frac{(IMAXx) \times \left(R_{Lx}\right)}{\left(IMAXx \times R_{Lx}\right) - v_x(t)} \right] + t_{SR} \quad (16)$$

where:

- R_{Lx} = the load resistance
- C_{Lx} = the load input capacitance (C_{LOAD1} or C_{LOAD2} in Figure 2)
- t_{SR} = the initial slow turn-on period, approximately 500 μs

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Equation 16 can be used to calculate the time it takes for either of the loads to charge completely by substituting that channel's parameters, and solving for t_{ST} when $v_x(t) = V_{DCx}$. However, if the secondary channel ramp turn-on is initiated by the primary channel's output voltage level, then the first period of interest is the time when the primary channel achieves the ramp-up command threshold. This time, designated t_{UP2} in equation 17, can be found from:

$$t_{UP2} = R_{L1} \times C_{L1} \times \ell n \left[\frac{IMAX_1 \times R_{L1}}{IMAX_1 \times R_{L1} - V_{RAMP}} \right] + t_{SR} \quad (17)$$

where:

- V_{RAMP} = the programmed ramp-up threshold established using equation 11, and the subscripted "1" indicates the primary, or controlling channel parameters

Once the controlled channel starts to turn on, its voltage ramp follows the same profile as the first channel. Therefore, the total start-up time for the sequenced outputs is given by equation 18.

$$t_{ST} = R_{L2} \times C_{L2} \times \ell n \left[\frac{IMAX_2 \times R_{L2}}{IMAX_2 \times R_{L2} - V_{DC2}} \right] + t_{UP2} + t_{SR} \quad (18)$$

where:

- V_{DC2} = secondary channel supply input voltage
- the subscripted "2" indicates the secondary, or controlled channel parameters

case 2: constant-current loads, no soft-start

Constant-current loads typically employ some type of undervoltage lockout (UVLO), or are achieved by holding processors and logic in reset until the supply has stabilized. Therefore, the ramp profile has two stages; the first stage from turn-on until the UVLO threshold (V_{UV} in the following equations) is reached, and the remaining period to ramp from V_{UV} to the steady-state level, V_{DC}. Once the load starts up, the input bulk capacitance is charged only by the sourcing current in excess of the load current.

Assuming the primary load starts up prior to its voltage attaining the slave channel ramp-up threshold ($V_{UV1} < V_{RAMP}$), the time to reach that threshold can be estimated from:

$$t_{UP2} = C_{L1} \times \left[\frac{V_{UV1}}{IMAX_1} + \frac{\left(V_{RAMP} - V_{UV1}\right)}{\left(IMAX_1 - I_{L1}\right)} \right] + t_{SR} \quad (19)$$

where:

- V_{UV1} = the master channel UVLO threshold
- V_{RAMP} = the controlled or slave channel ramp-up threshold
- I_{L1} = the master channel constant-current load

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With this known secondary-channel delay, the total start-up time can now be determined from the time at which the controlled channel reaches steady-state. This period is given by equation 20.

$$t_{ST} = C_{L2} \times \left[\frac{V_{UV2}}{IMAX_2} + \frac{\left(V_{DC2} - V_{UV2}\right)}{\left(IMAX_2 - I_{L2}\right)} \right] + t_{UP2} + t_{SR} \quad (20)$$

where:

- V_{UV2} = the slave channel UVLO threshold
- V_{DC2} = the slave channel supply input voltage

case 3: constant-current loads using soft-start

When soft-start is used to bring up a constant-current load, the ramp-up time determination becomes more complex. Prior to achieving its UVLO threshold, the primary channel's voltage profile is given by equation 21.

$$\nu_1(t) = \frac{\tau_{SS1} \times IMAX_1}{C_{L1}} \times \left[e^{\left(\frac{-\left(t - t_1\right)}{\tau_{SS1}} \right)} + \frac{\left(t - t_1\right)}{\tau_{SS1}} - 1 \right] \quad (21)$$

where:

- $\tau_{SS1} = R_{IMAX1} \times C_{SS1}$
- $t_1 = t_{SR}$ = the initial slow turn-on period, approximately 500 µs

Equation 21 can be plugged into a spreadsheet to solve iterively for different times of interest. Two useful time points are:

- the time $t = t_{UP2}$ when $\nu_1(t) = V_{RAMP}$, if $V_{RAMP} \leq V_{UV1}$ (V_{UV1} is the primary channel UVLO threshold), and
- the time $t = t_{VUV1}$ when $\nu_1(t) = V_{UV1}$, if $V_{RAMP} > V_{UV1}$

Assuming the UVLO threshold is less than the slave channel ramp-up threshold (case 2 above), the effect of the additional load can be factored into the voltage ramp profile. This better describes the second stage of the output ramp-up. Since the turn-on event of the second channel occurs during this stage, its point in time can be found by sampling voltage equation 22 for the time $t = t_{UP2}$ when $\nu_1(t) = V_{RAMP}$.

$$\nu_1(t) = \frac{1}{C_{L1}} \times \left[\tau_{SS1} \times IMAX_1 \times \left[e^{\frac{-\left(t - t_1\right)}{\tau_{SS1}}} - e^{\frac{-\left(t_{VUV1} - t_1\right)}{\tau_{SS1}}} \right] + \left(IMAX_1 - I_{L1}\right) \times \left(t - t_{VUV1}\right) \right] + V_{UV1} \quad (22)$$

where:

- t_{VUV1} is determined from equation 21

Note that for designs where $(t_{VUV1} - t_1) > 4 \times T_{SS1}$, the sourcing current has virtually attained the $IMAX_1$ level sometime prior to $t = t_{VUV1}$. From inspection of equation 22, it can be seen that the exponential terms become insignificant in this case. Therefore, a good approximation of the voltage waveform can be obtained by considering it to be the constant-current charging of C_{L1} at a rate of $(IMAX_1 - I_{L1})$. With this simplification, the time t_{UP2} can be calculated from equation 23.

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$$t_{UP2} \cong C_{L1} \times \left(\frac{V_{RAMP} - V_{UV1}}{IMAX_1 - I_{L1}} \right) + t_{VUV1} \quad (23)$$

Once the total delay to the secondary channel start-up (t_{UP2}) is known, substitution of the secondary channel parameters into equations 21 and 22 (or 23) can be used to determine the total system start-up time. Substitute τ_{SS2} for τ_{SS1}, $IMAX_2$ for $IMAX_1$, etc. However, for these calculations, the constant t_1 in equations 21 and 22 is now the quantity ($t_{UP2} + t_{SR}$). This version of equation 21 is used to determine the time at which the secondary channel load starts up, t_{VUV2} when $v_2(t) = V_{UV2}$. Finally, the system start-up time is calculated by substituting the secondary channel parameters into equation 22 (or 23) (including t_{VUV2} for t_{VUV1}) to model $v_2(t)$ when the output voltage is above the UVLO threshold.

setting the linear mode timeout

Once an estimate of the required charging time is obtained, the value of the timing capacitor C_T can be derived. Since the timeout is obtained via the constant-current charging of the external capacitor, the minimum capacitor value is given by:

$$C_{T(min)} = \frac{i_{CT(max)} \times t_{ST}}{V_{F(min)}} \cong \left[48 \times 10^{-6} \right] \times t_{ST} \quad (24)$$

where:

- $i_{CT}(MAX)$ = the maximum CT charging current, 65 μA
- $V_F(MIN)$ = the minimum fault threshold on the CT pin, 1.35 V

For the example application, a total start-up time of about 2.03 ms was obtained. Solving equation 24 using this timeout value produces a result of $C_T(MIN)$ = 0.097 μF; a 0.1-μF value is shown in the schematic.

using the FAULT output

LED indicator

The TPS2306 FAULT output provides fault reporting capability to the system host. It is an open-drain output which becomes high-impedance under any conditions which cause either of the GATE*x* outputs to be turned off. It can be used to provide a visual indication of a fault by using it as an LED pre-driver, as shown in Figure 7.

APPLICATION INFORMATION

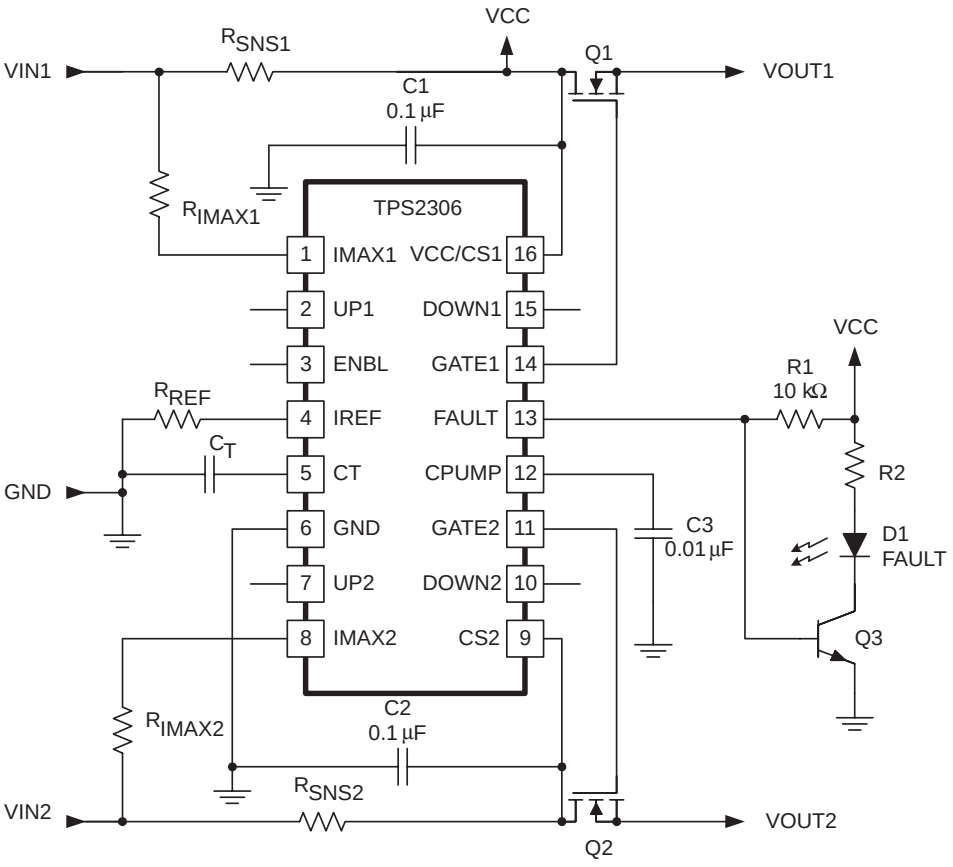


Figure 7. Possible FAULT LED Circuit

QuickSwitch® device

Another potential use of the FAULT output is to drive a bus isolation device, such as a Widebus™ or QuickSwitch® bus switch, as shown in Figure 8. The FAULT output can provide direct-drive of active low bus enable inputs of the switch device(s).

APPLICATION INFORMATION

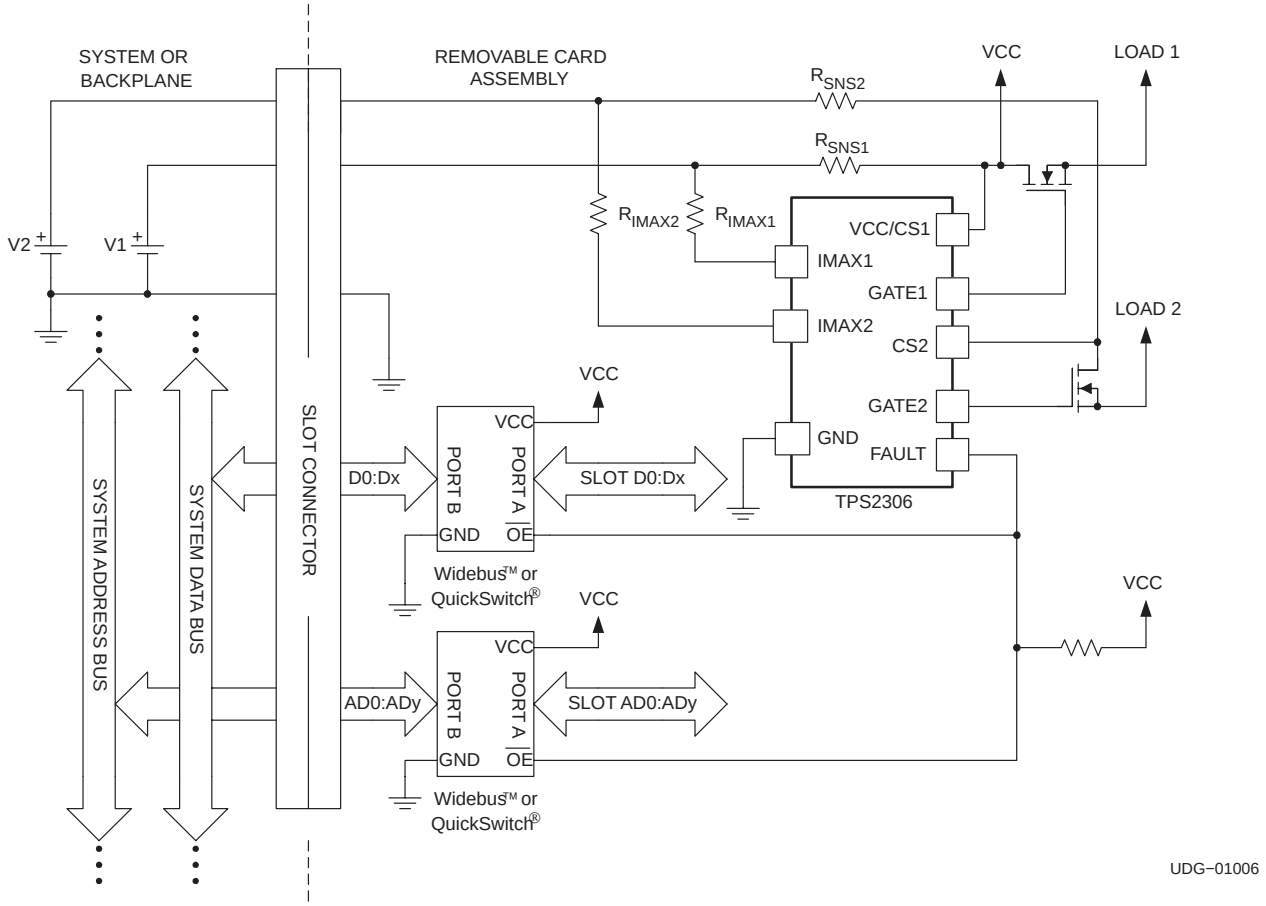


Figure 8. Using the TPS2306 with Bus Switches

With outputs disabled, the bus switches provide electrical isolation between the backplane and plug-in card buses. This is useful for reducing glitches on the system address and data busses during live insertions. Because of the linear mode detection of the TPS2306, the FAULT output remains asserted throughout the output voltage ramp period. This pin is not pulled low until a nominal delay after both output supplies have stabilized at the input voltage levels (see Figure 9). When this occurs, the slot and backplane busses are connected with a minimal impedance across the bus interface.

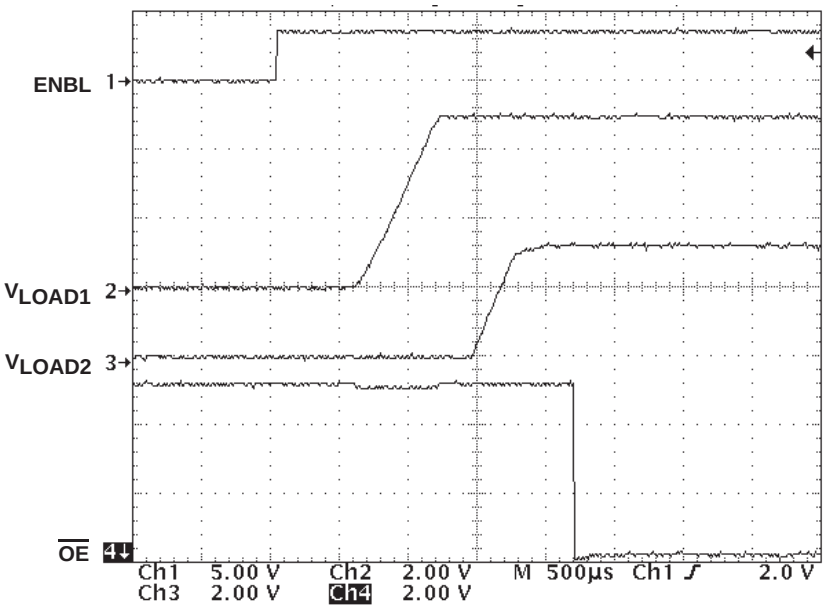


Figure 9. TPS2306 FAULT Operation During Ramp-Up

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS2306DW	NRND	SOIC	DW	16		TBD	Call TI	Call TI	Replaced by TPS2300IPW
TPS2306DWG4	NRND	SOIC	DW	16		TBD	Call TI	Call TI	Samples Not Available

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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